# PRE-STORED DIGTIAL WORD GENERATOR

## CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of U.S. application ser. no. 09/730998, filed on 7 Dec. 2000 and entitled "pre-stored digital word generator".

## FIELD OF THE INVENTION

The present invention is directed to a pre-stored digital word generator, and more particularly, to a digital word generator of a chip tester that employs an edge random access memory (RAM) to store the preset information of TG data so as to provide multiple digital words.

## BACKGROUND OF THE INVENTION

Reference is made to fig. 1, which is a schematic diagram of a conventional test channel inside a chip tester. In general, a conventional chip tester has multiple test channels for transmitting test vectors. For each channel, the tester needs to generate two kinds of data. One is F data and the other is TG data. F data are primary data for testing the device under test (DUT) 11 and TG data are trigger signals for triggering the signal generating circuit 10.

Reference is made to fig. 2, which is a schematic diagram of a conventional single digital word generator for producing TG data. As shown in the figure, the conventional single digital word generator has an edge-rising counter 102, an edge-falling counter 104 and a flip-flop component 12 (i.e. a latch component). The edge-rising counter 102 is used to preset the flip-flop component 12 to output a digital "1" (i.e. making the output of the flip-flop component 12 switch to high voltage) while the edge-falling counter 104 is used to clear the flip-flop

component 12 to output a digital "0" (i.e. making the output of the flip-flop component 12 switch to low voltage).

However, if the tester needs to provide TG data for multiple test channels or provide TG data with multiple pulses for a single test channel, it needs to employ a plurality of single digital word generators correspondingly. Hence, large number of word generators will be required. Since both of the edge-rising counter 102 and edge-falling counter 104 are made of multiple flip-flop components, which have large volume and are costly, it will cause the conventional tester bulky and expensive.

Accordingly, as discussed above, the prior art still has some drawbacks that could be improved. The present invention aims to resolve the drawbacks in the prior art.

## SUMMARY OF THE INVENTION

An objective of the present invention is to provide a pre-stored digital word generator to produce multiple digital words.

Another objective of the present invention is to provide a pre-stored digital word generator to reduce the cost of testing a digital device.

Still another objective of the present invention is to provide a pre-stored digital word generator to make easy to program the digital word generator.

In order to achieve the objectives above, the present invention provides a pre-stored digital word generator, which includes an edge memory used to store a primary preset information; an edge address counter used to point to an address of the edge memory; a reloadable down counter used to count according to the primary preset information and trigger the edge address counter; and a

plurality of word generating circuits having a secondary preset information, wherein the word generating circuits compares the primary and secondary preset information and then produce digital words for the signal generating circuits according to a comparison result.

Numerous additional features, benefits and details of the present invention are described in the detailed description, which follows.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will be more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a schematic diagram of a conventional test channel inside a chip tester.

Fig. 2 is a schematic diagram of a conventional single digital word generator for producing TG data.

Fig. 3 is a block diagram of a pre-stored digital word generator in accordance with the present invention.

Fig. 4 is a block diagram of a word generating circuit in accordance with the present invention.

Fig. 5 is a schematic diagram of a preferred embodiment for data arrangement of an edge RAM in accordance with the present invention.

Fig. 6 is a schematic diagram of an embodiment for data arrangement of registers in accordance with the present invention.

Fig. 7 is a waveform diagram of outputs of the pre-stored digital word

generator in accordance with the present invention.

## DETAILED DESCRIPTION

Reference is made to fig. 3, which is a block diagram of a pre-stored digital word generator in accordance with the present invention. It includes an edge random access memory (RAM) address counter 202, an edge RAM 204, a reloadable down counter 206 and multiple word generating circuits 28. Therein, as shown in fig. 4, the word generating circuits 28 each has a rise register 222, a fall register 224, a rising comparator 242, a falling comparator 244 and a flip-flop component 26.

The edge RAM 204 is used to store the preset information of TG data. An example of the preset information is shown in fig. 5. The present information for each address includes mark_count, mark_tag, rise_enable and fall_enable. In practice, a user can reset the edge RAM 204 easily. Hence, the present invention can make the digital word generator easy to program.

The edge RAM address counter 202 is used to count the memory address of the edge RAM 204. Every time when it is triggered by the reloadable down counter 206, it will point to the next address of the edge RAM 204.

Furthermore, every time when the reloadable down counter 206 counts down to zero, it will output a mark signal to trigger the edge RAM address counter 202 and word generating circuits 28. In addition, when the reloadable down counter 206 receives the mark_count information, it will be re-loaded by the mark_count information and then count accordingly. After finishing its counting, it will send out a mark signal again.

Each of the word generating circuits 28 is used to produce a digital word

according to the information received from the edge RAM 204. When it is triggered, it will use the rising comparator 242 and falling comparator 244 to compare the received information with the information stored in the registers 222 and 224 to determine whether the flip-flop component 26 should be preset or cleared so as to produce the digital word.

The information stored in the registers 222 and 224 are set by the tester when the tester needs to send out TG data. An example of the information stored in the registers of the word generating circuits 28 is shown in fig. 6.

In order to make the present invention clearer, reference is made to figs. 5-6 together with fig. 7, which is a waveform diagram of the output of the pre-stored digital word generator in accordance with the present invention. Initially, the edge RAM address counter 202 will point to address #0 of the edge RAM 204. Then, the corresponding information will be sent to the reloadable down counter 206 and the word generating circuits 28. The corresponding mark_tag, rise_enable and fall_enable information, i.e. "1", "1" and "0", will be sent to the word generating circuits 28 and the mark_count information, i.e. "2", will be sent to the reloadable down counter 206.

When received the mark_count information, i.e. "2" as shown in fig. 5, the reloadable down counter 206 will be re-loaded and then count backwards from two to zero. After finishing the counting, the reloadable down counter 206 will send out the first mark signal to make the edge RAM address counter 202 point to address #1 and trigger the word generating circuits 28.

At this moment, the word generating circuits 28 will use the rising comparator 242 and falling comparator 244 to compare the mark_tag

information, i.e. "1" as shown in fig. 5, received from the edge RAM 204 with the information stored in the registers 222 and 224 as shown in fig. 6. Take channel 1 for example. Since the information stored in the rise register 222 of channel 1 is "1", which is the same as the mark_tag value stored in address #0 of the edge RAM 204, and the rising comparator 242 of channel 1 is enabled by the rise_enable signal, i.e. "1" as shown in fig. 5, the rising comparator 242 of channel 1 will make the flip-flop component 26 switch to high voltage. Hence, at clock #2 shown in fig. 7, channel 1 starts to send a digital "1", i.e. a high-voltage signal.

Next, when the edge RAM address counter 202 counts to address #2, it will make the reloadable down counter 206 send out the third mark signal. At this moment, since the information stored in the fall register 224 of channel 1 is 3, which is the same as the mark_tag value stored in address #2 of the edge RAM 204, and the falling comparator 244 of channel 1 is enabled by the fall_enable signal, the falling comparator 244 of channel 1 will make the flip-flop component 26 switch to low voltage. Hence, at clock #6, channel 1 is changed to send a digital "0", i.e. a low-voltage signal. Since other operations of the word generating circuits 28 are the same as mentioned above, they won't be described in detail.

Summing up, the present invention has following features:

(1) The present invention can produce multiple digital words.

(2) Since the present invention uses fewer counters and hence has less flip-flop components, it can reduce the cost for testing a digital device.

(3) Since edge RAM can be reset arbitrarily, the present invention can be easily

programmed.

Although the present invention has been described with reference to the preferred embodiment thereof, it will be understood that the invention is not limited to the details thereof. Various substitutions and modifications have been suggested in the foregoing description, and other will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are embraced within the scope of the invention as defined in the appended claims.